Staff/Principal RTL Logic Design Engineer

Job Description

Responsibilities include (but not limited to):

- Engages with the architects to define design and verification requirements based on hardware functionality and requirements.
- Develop HW architecture from specification documents which include writing micro-architecture specifications and define efficient RTL modules and partition implementation.
- Performs all aspects of design tools and flows to qualify the logic implemented, such as RTL/DFx linting, clock/reset domain crossing check, synthesizability check to meet design quality, timing quality of the design, gate-count/power optimization, supporting verification team with debug and support physical design teams on timing constraints and other design topics using Verilog/System Verilog/VHDL.
- Develop and execute low power design (UPF/CPF).
- Design top level RTL, integration of blocks, clocks, resets, configuration registers, etc
- Knowledge of low-speed bus protocols (AMBA/OCP) and high-speed serial protocols (PCIe/USB/Ethernet) will used at various stages of the design.
- Awareness of DFT concepts to be used to fix functional violation that may get introduced which including DFT structures.
- Carry out static checks including Lint/CDC (Spyglass), synthesis, LEC and STA. Debugging and fixing functional break.
- Take ownership of tasks and drive tasks to closure.
- Provides technical direction, guidance and support to the IP development team and stakeholders throughout the Product Life Cycle.

Minimum Qualifications:

Possess a Bachelor's, a Master's degree or a Ph.D. in Electronics Engineering, Computer Engineering, or equivalent and experience with IP/SoC design or verification development.

- At least 8 years of relevant working experience in Silicon Logic Design or verification development.
- Strong fundamental in Logic (RTL) using VHDL / Verilog / System Verilog.
- Exposure to micro-processor integration is an added advantage
- Experience of working with Analog Mixed Signal design team is an advantage
- Strong technical leader who communicates well with great influencing skills.
- Strong analysis, debugging skills, and creative in problem solving.
- Motivated, Self-driven and Independent
- Experience in any of these design tools and methodologies is/are an added advantage:
- System Verilog (OVM/UVM)
- Scripting (Python/Perl/Shell)
- Interactive debugger
- RTL model build
- Testbench development
- Power-aware simulation
- Coverage-based random constraint simulation
- Formal Property Verification
- Power Management
- Design For Test/Verification (DFT/DFV/DFX)
- USB, PCI-Express specifications
- Any industry standard device OR interface protocol