ASIC Physical Design Engineer

Job Description:

Responsibilities include (but are not limited to):

- You will be participating in the leading-edge System-On-a-Chip (SoC) design projects using cutting-edge process technology nodes for various client applications.
- Ideate, develop, and execute physical design solutions: floorplan, placement, routing, cell sizing, buffering, logic restructuring to improve timing and power.
- Participate in design/architecture reviews to track design milestones.
- Evaluate and deploy the evolving physical design methodologies to handle increasingly complex SoC/IP designs within aggressive, market-driven schedules.
- Active participation in benchmarking of library, technology parameters, and implementation strategy to enable design requirements of die size, power & speed.
- Actively work as part of a team both locally and with remote or multi-site teams.
- Actively assists full chip timing constraints development, full chip Static Timing Analysis, and timing signoff for a complex, multi-clock, multi-voltage SoC.
- Analyze and incorporate advance timing signoff flows (SSTA, LOCV Based STA, IR Drop aware STA) into SoC timing signoff flow.
- Active participation to enhance the flow from the front end (pre-layout) to the back end (post-layout) at both chip level and block level.

Key Requirements:

- Minimum of a Bachelor's Degree in Electrical and/or Electronics Engineering, Computer Engineering, or any related discipline.
- Good understanding of Digital Logic, VHDL/RTL representation, Verilog
- Good scripting skills in Perl, Tcl, Python to handle and optimize CAD automation flow
- Experience with Synopsys EDA tools: Fusion Compiler, Primetime, IC Validator, VC Low-Power
- Experience with Cadence EDA tools: Innovus, Tempus, Virtuoso, Conformal Low-Power

Additional Skills:

- Experience in advance FinFET process nodes and below (16nm, 12nm, 7nm, 5nm, 3nm), including low-power methodology
- Expertise in analyzing and converging crosstalk delay, noise glitch, and electrical/manufacturing rules in deep-sub-micron processes.
- Hands-on experience in full-chip or sub-chip Static Timing Analysis, timing constraints management, and timing closure.