Senior SoC Physical Design Engineer

We are seeking an experienced Senior SoC Physical Design Engineer proficient in Mandarin, with a minimum of 5 years in physical design. The ideal candidate will be responsible for executing RTL-to-GDSII implementations and ensuring all signoff checks are completed for advanced System-On-a-Chip (SoC) projects.

Job Description:

Responsibilities include (but are not limited to):

- Perform physical design implementation from RTL to GDSII, including tasks such as synthesis, floorplanning, placement, routing, and clock tree synthesis.
- Conduct verification and signoff procedures, including Static Timing Analysis (STA), physical layout verification, power integrity, and reliability assessments.
- Collaborate with architecture and design teams to define and generate timing specifications, clocking strategies, and constraints.
- Analyze timing reports, automate tasks using scripting languages, and provide timely feedback for timing ECOs.
- Participate in the development and enhancement of physical design methodologies and flow automation to optimize design performance.

Key Requirements:

- Bachelor's or Master's degree in Electrical Engineering, Electronics Engineering, Computer Engineering, or a related field.
- Minimum of 5 years of experience in SoC physical design.
- Fluency in Mandarin (spoken) is required.
- Experience with EDA tools such as Synopsys Fusion Compiler, PrimeTime, IC Validator, and RedHawk.
- Strong scripting skills in languages like Perl, Tcl, or Python for CAD automation.
- Hands-on experience with advanced process nodes (10nm and below) and low-power design methodologies.
- Expertise in high-speed design and resolving issues related to crosstalk delay, noise glitches, and deep-sub-micron electrical/manufacturing rules.
- Proficiency in digital logic design and RTL coding (VHDL/Verilog) will be an added advantage.