Lead Design Verification Engineer

Job Description

Responsibilities include (but are not limited to):

- Develop and execute comprehensive verification plans for complex IP, ASIC, and SoC designs.
- Create, simulate, and debug testbenches using Verilog/SystemVerilog and UVM methodologies.
- Collaborate with design teams to ensure design quality and functionality.
- Analyze functional and code coverage metrics to identify verification gaps and improve test efficiency.
- Conduct gate-level and post-silicon simulations to verify design performance and reliability.
- Utilize scripting languages (Python, Perl, TCL, or Shell) to automate verification tasks and improve productivity.

Requirements

- Bachelor's or Master's degree in Electrical Engineering, Computer Science, or a related field.
- Minimum of 6 years of hands-on experience in pre-silicon verification.
- Strong proficiency in Verilog/System Verilog and UVM.
- In-depth understanding of functional coverage and code coverage improvement techniques.
- Proven experience in gate-level and post-silicon verification.
- Excellent problem-solving and analytical skills.
- Strong communication and teamwork abilities.
- Proficiency in at least one scripting language (Python, Perl, TCL, or Shell).
- Knowledge in AXI. AMBA protocols.
- Experienced in PCIe or USB IP-level verifications.