Logic Design Engineer

Job Description

Responsibilities include (but are not limited to):

- Engages with the architects to define design and verification requirements based on hardware functionality and requirements.
- Develops micro-architecture specifications and writes efficient and elegant RTL to implement features.
- Executes RTL simulation and integration, timing convergence, formal verification, ECO implementation, debug analysis and reviews.
- Performs all aspects of design tools and flows to qualify the logic implemented, such as RTL/DFx linting, clock/reset domain crossing check, synthesizability check to meet design quality, timing constraint definition and review, gate-count/power optimization, etc.
- Provides technical direction, guidance and support to the IP development team and stakeholders throughout the Product Life Cycle.

Requirements

- Minimum of a Bachelor's degree in Electronic/Electrical Engineering, Computer Engineering, or equivalent.
- Minimum 3 years of experience of related field.
- Strong analysis, debugging skills, and creative in problem solving.
- Motivated, Self-driven and Independent.
- Well verse in System Verilog (OVM/UVM), Scripting (Python/Perl/Shell), RTL simulators, Interactive debugger, RTL model build, Testbench development, Power-aware simulation, Coverage-based random constraint simulation, Formal Property Verification