Analog IC Layout Design Engineer

Job Description

Responsibilities include (but are not limited to):

- Work and lead junior engineer towards projects delivery with other layout and circuit design engineers to resolve any technical issues that will affect layout to ensure high quality.
- Utilize EDA tools (Cadence and Synopsys) for layout design and all related verification items, perform all layout activities as cell and block level creation, edit and full verification.
- Use state-of-the-art layout techniques for matching, ESD, latch-up prevention and parasitic reduction and work with an awareness and understanding of the process from physical point of view.
- Attending all relevant project meetings, continuous assessment and reporting of timescale risks.
- Where possible, use schematic driven layout and consider top level auto routing.
- Involve in review session and prepare all related document and data preparation for wafer tape out.

Requirements

- Bachelor's Degree Engineering in Electrical/Electronic, Physics, Computer or related fields.
- Must have Good verbal and written communication skills in English. Japanese is a plus
- Thorough understanding of integrated analog circuit design
- Thorough understanding of chip layout in cell and block level creation, edit and full verification.
- Experience with layout techniques for matching, ESD, latch-up prevention and parasitic reduction and work with an awareness and understanding of the process from physical point of view.
- Experience in analog IC/ mixed signals IC layout designs and verifications. Able to perform with ideas on chip size reduction.
- Highly self-motivated and adaptable.
- Having the basic knowledge of CMOS related devises including high voltage and the skill of deciphering Design Manual.