Design For Testability (DFT) Engineer

This job description outlines the responsibilities and skills required for a Design For Testability (DFT) Engineer.

Responsibilities:

- Implement and apply DFT techniques to ensure efficient testing of integrated circuits (ICs).
- Develop and analyze test patterns using tools like Tessent or TetraMax for:
    - **ATPG (Automatic Test Pattern Generation):** Generating test cases to identify manufacturing defects.
    - **Compression:** Reducing the size of test data for efficient application.
    - **MBIST (Memory Built-in Self Test):** Designing embedded test logic for memory components.
    - **PBIST (Physical Built-in Self Test**): Testing various physical components within an IC.
- Perform scan stitching using tools like DC, FC, or Tessent to connect scan chains for efficient testing.
- Analyze Design Rule Checks (DRCs) and identify potential manufacturing issues, proposing solutions to address them.
- Run and analyze timing and non-timing simulations to verify test pattern functionality and identify potential timing violations.
- May contribute to scripting automation using TCL or Perl for improved efficiency.

Requirements:

- Experience in MBIST and PBIST (Physical Built-in Self Test) methodologies.
- Expertise in scan stitching using industry-standard tools.
- Proficiency in ATPG, compression, and MBIST using tools like Tessent or TetraMax.
- Experience with timing and non-timing simulations.
- Ability to analyze and resolve DRC violations.
- Familiarity with scripting languages like TCL or Perl is a plus.