Design Verification Engineer

Job Description

Responsibilities include (but are not limited to):

- Defines and implements verification procedures for IP Hardware product based on features, requirements, and failure points.
- Creates initial product verification methodology, selecting the verification strategy, identify failure points and developing test plans.
- Develops verification environments and collaterals such as testbenches, stimulus/sequences, checkers, assertions, and coverage.
- Performs tests regression, collects and analyzes regression results, root-causes and resolves regression failures.
- Provides technical direction, guidance and support to the IP development team and stakeholders throughout the Product Life Cycle.
- Influences on product development execution efficiency and quality through continuous improvement on verification methodologies and strategies used across product families.

Requirements

- Minimum of a Bachelor's degree in Electronic/Electrical Engineering, Computer Engineering, or equivalent.
- Minimum 3 years of experience of related field.
- Strong analysis, debugging skills, and creative in problem solving.
- Motivated, Self-driven and Independent.
- Well verse in System Verilog (OVM/UVM), Scripting (Python/Perl/Shell), RTL simulators, Interactive debugger, RTL model build, Testbench development, Power-aware simulation, Coverage-based random constraint simulation, Formal Property Verification