IC Design Engineers Junior/ Senior/ Staff/ Principal (Kuching, Sarawak)

We are hiring for all design positions: Logic Design, Design Verification Engineers, AMS Circuit Design Engineers, and Physical Design Engineers. In these positions, you will be participating in leading-edge ASIC (Application Specific IC) and System-On-a-Chip (SoC) designs.

A) Logic Design & Validation Engineers

Responsibilities include (but are not limited to):

- Engages with the architects to define design and verification requirements based on hardware functionality and requirements.
- Develop HW architecture from specification documents which include writing micro-architecture specifications and defining efficient RTL modules and partition implementation
- Performs all aspects of design tools and flows to qualify the logic implemented, such as RTL/DFx linting, clock/reset domain crossing check, synthesizability check to meet design quality, timing quality of the design, gate-count/power optimization, supporting verification team with debug and support physical design teams on timing constraints and other design topics using Verilog/System Verilog/VHDL.
- Develop and execute low power design (UPF/CPF).
- Design top-level RTL, integration of blocks, clocks, resets, configuration registers, etc
- Awareness of DFT concepts to be used to fix functional violation that may get introduced which including DFT structures.
- Carry out static checks including Lint/CDC (Spyglass), synthesis, LEC and STA. Debugging and fixing functional break.
- Verifying designs including functional tests development and validations

Requirements

Possess a Bachelor's, a Master's degree or a Ph.D. in Electronics Engineering, Computer Engineering, or equivalent and experience with IP/SoC design or verification development.

- Familiarity with digital electronic designs and hardware description languages (for example, Verilog, VHDL)
- Familiarity with one or more VLSI logic design/verification languages example System Verilog, VERA, Specman, SystemC and Testbuilder .
- Familiarity with one or more VLSI logic design/verification flows example VMM, OVM, RVM and AVM and relevant EDA tools.
- Familiarity with one or more industry-standard bus interfaces and protocols (for example, PCI Express, SATA, AMBA, and others)
- Scripting (Python/Perl/Shell)
- Experience in leading a technical team would be an added advantage.

B) Analog Mixed Signal Circuit Design Engineers

Responsibilities include (but are not limited to):

- Responsible for the latest industry logic process technology, digital & analog circuit design for the next generation of high-speed and low-power circuit solutions.
- Develop Analog Interface IPs such as Data Converters (A/D, D/A), Phase Locked Loop (PLL), High-Speed Serial Interface PHY, DDR PHY, and reference circuits with emphasis on high-speed applications. Involve in the transistor-level design and development of high-speed interfaces such as Serdes, PLL, USB PHY, PCIe PHY, DAC, special I/O buffer, transmitter & receiver circuit.
- Take charge of Key IP developments for analog/mixed-signal IC design projects;
- Engage with other team members to establish design requirements and IP specifications. Provide technical support to more junior members of the team.
- Provide technical guidance to layout, application, and evaluation teams;
- Deliver design documents, including the design specifications, review forms, and evaluation plans;
- Definition, design, simulation, verification, and documentation of high-performance mixed-signal integrated circuits;
- Responsible for all activities ranging from architecture and design to silicon bring-up and characterisation;
- Collaborate with Applications, Process Technology, CAD, Test, Reliability, Marketing and Product Engineering;
- Define, coordinate, and conduct design verification tests to ensure compliance with customer, environmental, and regulatory requirements. • Supports customer application questions and issues.

Requirements

Possess a Bachelor's, a Master's degree or a Ph.D. in Electronics Engineering, Computer Engineering, or equivalent with experience in analog and mixed-signal design

- Knowledge of semiconductor device physics and advance process technology. Experience in circuit design, circuit simulation and custom layout design using industry EDA tools i.e. Synopsys, Cadence or Mentor.
- Proficiency in the design of building blocks, such as IOs, Converters – A/D and D/A, high-speed op-amps, comparators, clock distribution elements, reference voltage, and current source circuits.
- Experience in high-speed analog and mixed-signal design, architecture, system and integration aspects for A/D and D/A converters, PLLs, DDR, MIPI and HBM PHYs or other similar standards is an added advantage
- Scripting/software writing skills would be an added advantage.

C) Physical Design Engineers

Responsibilities include (but are not limited to):

- Defining VLSI physical design implementation methodology and developing design flows
- Implementing physical designs, such as floor planning, power-grid and clock tree designs, timing budgeting, place and route, RC-extraction and integration
- Full chip timing constraints development, full chip Static Timing Analysis, and Signoff for a complex, multi-clock, multi-voltage SoC
- Analyze and incorporate advance timing signoff flows (SSTA, LOCV Based STA, IR Drop aware STA) into SoC timing signoff flow.
- Active participation to enhance the flow from the front end (pre-layout) to the back end (postlayout) at both chip level and block level.
- Verifying physical designs, such as functional equivalency, timing/performance, noise, layout rules, reliability and power

Requirements

Possess a Bachelor's, a Master's degree or a Ph.D. in Electronics Engineering, Computer Engineering, or equivalent with the below knowledge (but not limited to):

- Good level of understanding and hands-on experience in Very Large Scale Integration (VLSI) design and physical design implementation
- Knowledge of semiconductor device physics and advanced process technology. Experience in ASIC Physical Design using industry EDA tools i.e. Synopsys, Cadence, or Mentor
- Prior experience in timing closure, clock/power distribution and analysis, RC extraction, and correlation.
- Hands-on experience in full-chip/sub-chip Static Timing Analysis, timing constraints generation and management, and timing convergence.
- Expertise in physical design and optimization: floorplan, placement, routing, cell sizing, buffering, logic restructuring to improve timing and power. • Expertise in analyzing and converging crosstalk delay, noise glitch, and electrical/manufacturing rules in deep-sub-micron processes
- Understanding of process variation effect modeling and experience in design convergence taking into account variations.
- Experience in critical path planning and crafting.
- Scripting (Python/Perl/Shell)