ASIC Physical Design Engineer

Job Description

Responsibilities include (but not limited to):

- You will be participating in the leading-edge System-On-a-Chip (SoC) design projects using cutting-edge process technology nodes for various client applications.
- Ideate, develop, and execute physical design solutions.
- Participate in design/architecture reviews.
- Evaluate and deploy the evolving physical design methodologies to handle increasingly complex SoC/IP designs within aggressive, market-driven schedules.
- Active participation in benchmarking of library, technology parameters, and implementation strategy to enable design requirements of die size, power & speed.
- Enable technological innovations from day-to-day learning and project experiences.
- Actively work as part of a team both locally and also with remote or multi-site teams.
- Macroblock and chip level floor planning of digital logic, memories, IO's.
- Full chip timing constraints development, full chip Static Timing Analysis, and Signoff for a complex, multi-clock, multi-voltage SoC.
- Analyze and incorporate advance timing signoff flows (SSTA, LOCV Based STA, IR Drop aware STA) into SoC timing signoff flow.
- Active participation to enhance the flow from the front end (pre-layout) to the back end (post-layout) at both chip level and block level.

Minimum Qualifications:

- Minimum of a Bachelor's degree in Electrical and/or Electronics Engineering, Computer Engineering, or any related discipline.
- Good level of understanding and hands-on experience in Very Large Scale Integration (VLSI) design and physical design implementation.
- Prior experience in timing closure, clock/power distribution and analysis, RC extraction, and correlation.
- Hands-on experience in full-chip/sub-chip Static Timing Analysis, timing constraints generation and management, and timing convergence.
- Expertise in physical design and optimization: floorplan, placement, routing, cell sizing, buffering, logic restructuring to improve timing and power.
- Expertise in analyzing and converging crosstalk delay, noise glitch, and electrical/manufacturing rules in deep-sub-micron processes
- Understanding of process variation effect modeling and experience in design convergence taking into account variations.
- Experience in critical path planning and crafting.